R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a selected phase of a first clock signal and (ii) two or more serial data signals. The second circuit may be configured to present the two or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims may be found in the specification on page 8, line 19, through page 10, line 12. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-16 under 35 U.S.C. §103(a) as being over Tabata '345 in view of Mullaney et al. '575 is respectfully traversed and should be withdrawn.

Tabata et al. teaches a method and apparatus for enlarging/reducing two-dimensional images (Title). Mullaney

teaches a high speed cross point switch routing circuit with a word-synchronous serial back plane (Title).

In contrast, the present invention provides a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a first clock signal and (ii) two or more serial data signals. A second circuit may be configured to present the two or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

While difficult to understand, it appears that the Examiner is reading the circuits 1402 and 1403 of Tabata as the claimed first circuit and the elements 1404, 1405, 1406 and 1407 of Tabata as the claimed second circuit. As discussed in the Office Action, the so-called first circuit of Tabata does not appear to present a clock signal, as presently claimed. For example, FIG. 4 of Tabata is silent regarding any clock signals. Therefore, Tabata on its face does not teach or suggest each of the elements of the present claims. Furthermore, Mullaney does not cure the deficiencies of Tabata. In particular, none of the clock signals of Mullaney appear to be a selected phase of a first clock signal, as presently claimed. As such, Mullaney does not teach or suggest the selected phase of the first clock signal.

In conclusion, Tabata, alone or in combination with Mullaney, do not teach or suggest a first circuit configured to

present a parallel output data signal in response to (i) a selected phase of a first clock signal and (ii) two or more serial data signals. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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